Client's ref.: NTC-91198/吳昌榮等
File: 0548-9346usf/Jacky/Steve

TITLE

METHOD OF REDUCING THE ASPECT RATIO OF A TRENCH

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor manufacturing process, and more particularly, to a method of reducing the aspect ratio of a trench.

Description of the Related Art

Semiconductor device geometry continues to decrease in size, providing more devices per fabricated wafer. Currently, some devices are fabricated with less than 0.25μm spacing between features; in some cases there is as little as 0.18μm spacing between features, which often takes the form of a trench.

An isolation technique called shallow trench isolation (STI) has been introduced to the fabrication of devices to reduce size. Isolation trenches are formed in a substrate between features, such as transistors. Figs. 1A~1B are schematic views of a traditional STI process.

In Fig. 1A, a substrate 10 such as a silicon wafer is provided. A shield layer 11 composed of a pad oxide layer 12 and a silicon nitride layer 14 is formed on part of the substrate 10. The shield layer 11 serves as a stacked mask defining an isolation area in the substrate 10. The pad oxide layer 12 can be a SiO_2 layer with a thickness of 50~150Å, formed by chemical vapor deposition (CVD) or thermal oxidation. The silicon nitride layer 14 can be a Si_3N_4 layer with a thickness of 800~1500Å, formed by CVD.

In Fig. 1B, using the shield layer 11 as a mask, part of the substrate 10 is etched to form a trench 15. A thin oxide film 16, serving as a linear layer, is then formed by thermal oxidation, conformal to the surface of the trench 15. The thickness of the thin oxide film 16 is about 180~220Å. Next, a trench-filling material such as a SiO_2 layer 18 is deposited in the trench 15 once with a conventional high-density plasma chemical vapor deposition (HDP-CVD). Typically, the HDP-CVD reaction gas includes O_2 and silane (SiH_4).

Fig. 1C shows that a void may form when a trench with a narrow gap is filled by traditional process. For example, when the width of the trench 15 is less than 0.15μm and/or the aspect ratio of the trench is greater than 4, a void 20 is easily formed in a SiO_2 layer 19 with the traditional process. Such a void 20 seriously affects device reliability and yield, and hinders reduction in semiconductor device geometry.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a method of forming a shallow trench isolation (STI) in a substrate.

Another object of the present invention is to provide a method for lowering the aspect ratio of a trench during a deposition process to fill the trench without creating voids.

In order to achieve these objects, the present invention provides a method of reducing the aspect ratio of a trench. A trench is formed in a substrate. A conformal first insulating layer is formed on a surface of the trench. A conformal second insulating layer is formed on the first insulating layer. A conformal third insulating layer is formed on the second

insulating layer. The first, second and third insulating layers are anisotropically etched to form a remaining first insulating layer on a sidewall of the trench, a remaining second insulating layer on the remaining first insulating layer and a remaining third insulating layer on the remaining second insulating layer. By performing an etching procedure, the remaining third insulating layer is removed at a third etching rate, part of the remaining second insulating layer is removed at a second etching rate and part of the remaining first insulating layer is removed at a first etching rate. The third etching rate is greater than the second etching rate and the second etching rate is greater than the first etching rate.

The present invention improves on the prior art in that the present method forms an insulating spacer on the sidewall of the trench and thus produces a triple "U" shaped trench rather than the conventional single "U" shaped trench. Thus, the invention can reduce the aspect ratio of the trench, thereby preventing void formation during trench filling and ameliorating the disadvantages of the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

Figs. 1A~1B are sectional views according to the conventional STI process;

Fig. 1C is a schematic view, according to the conventional STI process, that forms a void in a trench; and

Figs. 2~9 are sectional views according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention will now be described in detail with reference to the accompanying drawings. Figs. 2~9 are sectional views showing the trench isolation process of the present invention.

In Fig. 2, a semiconductor substrate 200, such as a silicon wafer, is provided. A shield layer 205 preferably composed of a pad oxide layer 210 and a silicon nitride layer 220 is formed on part of the substrate 200. The pad oxide layer 210 can be a SiO_2 layer formed by thermal oxidation or CVD (chemical vapor deposition). The silicon nitride layer 220 can be a Si_3N_4 layer formed by CVD. For example, the thickness of the pad oxide layer 210 is about 100Å and the thickness of the silicon nitride layer 220 is about 900Å. The shield layer 205 serves as a stacked mask for defining an isolation area in the substrate 200.

In Fig. 3, using the shield layer 205 as a mask, part of the substrate 200 is etched to form a trench 310. The depth of the trench 310 is, for example, 2600~5000Å. Moreover, a thin oxide film (not shown), such as a SiO_2 film, can be conformably formed on the side and the bottom of the trench 310 by thermal oxidation. The thin oxide film (not shown) serves as a linear layer of about 180~220Å in thickness. In order to simplify the illustration, the thin oxide film (or the linear layer) is not shown in Figs.2~9.

In Fig. 4, using HDP-CVD, a conformal Si-rich oxide layer 410 is formed on the surface of the trench 310. The thickness of the Si-rich layer 410 is about 50~100Å.

In Fig. 4, using HDP-CVD, a conformal first silicon oxide layer 420, such as a SiO_2 layer, is formed on the Si-rich oxide layer 410. The thickness of the first oxide layer 420 is about 100~120Å.

In Fig. 4, using low pressure chemical vapor deposition (LP-CVD), a conformal second silicon oxide layer 430, such as a TEOS-SiO_2 layer, is formed on the first silicon oxide layer 420. That is, the LP-CVD reaction gas can be TEOS (tetra-ethyl-ortho-silicate). The thickness of the second oxide layer is about 100~150Å.

In Fig. 5, the Si-rich oxide layer 410, the second oxide layer 420 and the first oxide layer 430 are partially etched back by anisotropic etching. Thus, a remaining Si-rich oxide layer 410' is left on the sidewall of the trench 310, a remaining first silicon oxide layer 420' is left on the remaining Si-rich layer 410' and a remaining second silicon oxide layer 430' is left on the remaining first silicon oxide layer 420'. The above described step forms a multi-oxide spacer on the side surface of the trench 310, wherein the multi-oxide spacer is composed of a remaining Si-rich oxide layer 410', a remaining second oxide layer 420' and a remaining first oxide layer 430'. The anisotropic etching can be a plasma etching procedure using CF_4-containing gas. It should be noted that the remaining Si-rich oxide layer 410', the remaining first silicon oxide layer 420' and the remaining second silicon oxide layer 430' are lower than the top surface of the substrate 200.

In Fig. 6, by etching with a buffer oxide etcher (BOE) solution, the remaining second silicon oxide layer 430' is removed at a third etching rate, part of the remaining first silicon oxide layer 420' is removed at a second etching rate and part of the remaining Si-rich oxide layer 410' is removed at a first etching rate. The etching procedure can be performed at a time mode. The third etching rate is greater than the second etching rate and the second etching rate is greater than the first etching rate. Accordingly, a triple "U" shaped trench is formed and thus reduces the trench aspect ratio.

For example, the etching procedure uses a BOE solution consisting of NH_4F(40%), HF(49%) and dionized water (DI). The volume ratio of NH_4F/HF/DI is about 5/1/48. The third etching rate is about 800Å/min, the second etching rate is 400Å/min and the first etching rate is 200Å/min. The etching time is about 30 seconds.

Here, a demonstration of the present invention is provided, illustrating the reduced trench aspect ratio. Subsequent to the present process, referring to Fig. 6, it is assumed that: P=1000Å, w1=500Å, w2=700Å, w3=800Å, h1=1100Å, h2=100Å, h3=2700Å.

The original aspect ratio (AR)

= (h1+h2+h3)/w3 = 3900/800

= 4.87

Subsequent to the present process, the aspect ratio (AR')

= AR*(w3*h1+w2*h2+w1*h3)/w3*(h1+h2+h3)

= 4.87*[(800*1100+700*100+500*2700)/ (800*3900)]

= 4.87*0.737

= 3.59

Next, referring to Fig. 7, using HDP-CVD or TEOS-CVD, the trench 310 is filled with an insulation layer 710 extending onto the shield layer 205. The insulation layer 710 is, for example, a SiO_2 layer. Due to the lower aspect ratio of the trench 310 according to the present method, void-free deposition is easily achieved.

In Fig. 8, a planarization such as chemical mechanical polishing (CMP) is performed on the insulation layer 710 to produce a smooth insulation layer 710', wherein the shield layer 205 serves as a stop layer for the planarization.

In Fig. 9, the silicon nitride layer 220 is removed by, for example, a phosphoric acid solution. The pad oxide layer 210 is removed by, for example, an HF solution. Thus, a void-free STI profile 910 is formed.

Thus, the present invention provides a method of forming void-free STI in a substrate, and a method of lowering the aspect ratio of a trench during a deposition process filling the trench. Additionally, the present invention significantly improves the reliability of the product and achieves the goal of IC reduction.

Finally, while the invention has been described by way of example and in terms of the above, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.